Q.P. Code: **16EC5508** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester (R16) Regular Examinations January 2017

HARDWARE SOFTWARE CO-DESIGN

(VLSI)

(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 = 60** Marks)

UNIT-I

Q.1	a.	Outline the role of language in co-design.	2M
	b.	Discuss various steps involved in generic Co-design methodology using flow diagram	10M
		OR	
Q.2	a.	Write short notes on distributed system co-synthesis	4M
	b.	Demonstrate FSMD model for capturing the behavior of Co-synthesis system using an example	8M
		UNIT-II	
Q.3	a.	Describe an architecture that can be used in control dominated applications	6M
	b.	Write short notes on mixed and less specialized systems	6M
		OR	
Q.4	a.	Present different design flow integrations for emulation	8M
	b.	Identify different memory component specialization techniques	4M
		UNIT-III	
Q.5	a.	Discuss practical considerations in a Compiler Development Environment for embedded systems	6M
	b.	Discuss various compiler validation techniques	6M
		OR	
Q.6	a.	Describe traditional steps in compilation	6M
	b.	Elucidate concept of retargetable compiler	6M
		UNIT-IV	
Q.7	a.	Discuss about Optimization for embedded processors	6M
	b.	Categorize and discuss concurrent computations in detail	6M
		OR	
Q.8	a.	Discuss about design representation for system level synthesis.	6M
	b.	Classify coordinating concurrent computation mechanisms	6M
		UNIT-V	
Q.9	a.	Discuss various system level specification schemes	6M
	b.	Outline COSYMA Hardware Architecture	6M
		OR	
Q.10	a.	Contrast Master slave to distributed co-simulation models	6M
	b.	List approaches for multi-language validation	6M

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